and oxynitride layers on the polysilicon layer and then structuring the polysilicon layer and protective layer to form the gate path.--

--12. A method according to claim 11, wherein the protective layer is formed with a thickness so that the protective layer exhibits a thickness of less than 100nm after the structuring step.--

--13. A method according to claim 11, which includes, after the step of forming sacrificial contacts and prior to the step of preparing contacts to the predetermined source/drain regions, removing the protective layer from the gate paths, at least in the first region, and then doping the gate paths in the first region with a dopant having different conductive types.--

--14. A method according to claim 13, which includes, after the step of doping the gate paths in the first region, generating a silicide layer on the doped gate paths of the first region of the semiconductor substrate.--

--15. A method according to claim 14, wherein the silicide layer is selected from silicides consisting of $CoSi_2$, $TaSi_2$, $TiSi_2$ and WSi_x.--

--16. A method according to claim 15, wherein the step of generating a silicide comprises the step of providing a metal selected from Co, Ta, Ti and W on the gate paths of the first region and subsequently heating to convert the metal into a metal silicide layer.--

(Cont.)

--17. A method according to claim 14, wherein the step of generating a silicide layer on the gate paths of the first region includes applying a metal capable of forming a silicide onto the gate paths of the first region and subsequently heating to create the silicide layer.--

--18. A method according to claim 9, which includes, prior to the step of forming contacts to the predetermined source/drain region of the second region, generating silicide layers on the gate paths of the first region of the semiconductor substrate.--